

What is claimed is:

1 1. A fault tolerant computer comprising: a processor to execute
2 instructions, said processor including instructions to execute an original and
3 mirror instructions to produce results to be compared in a redundancy routine, a
4 radiation hardened comparison circuit coupled to compare an original result and
5 a first mirror result, said comparison circuit providing an output of a first state
6 when said original result agrees with said mirror result and an output of a second
7 state when said original result and said mirror result disagree, said second state
8 comprising an SEU error signal.

1 2. A fault tolerant computer according to claim 1 wherein absence of an
2 original or mirror result comprises disagreement with the other result.

1 3. A fault tolerant computer according to claim 1 wherein said comparison
2 circuit output is coupled to inhibit production of additional mirror results when said
3 output is in the first state.

1 4. A fault tolerant computer according to claim 3 wherein said processor
2 is provided with instructions to perform an SEU recovery routine in response to
3 detection of an SEU error signal.

1 5. A fault tolerant computer according to claim 4 wherein said processor
2 comprises means for storing the original result and the mirror result in response
3 to an SEU error signal, means coupling the SEU error signal to command
4 production of a next original result and a next mirror result, coupling means
5 coupling said original result for comparison with said next original result by said
6 comparison circuit and coupling said mirror result for comparison with said next
7 mirror result by said comparison circuit and said comparison circuit comprising
8 means for producing a signal of the first state when at least one of the original
9 result and next original result or the mirror result and next mirror result match to
10 allow use of a result matching a next result by said processor.

1 6. A fault tolerant computer according to claim 5 wherein allowing use
2 comprises transmitting the result to a processor bus.

1 7. A fault tolerant computer method comprising: executing an original
2 and mirror instructions to produce an original and a mirror result respectively to
3 be compared in a redundancy routine, comparing said original and mirror results
4 in a radiation hardened comparison circuit, and providing an output of a first state
5 when said original result agrees with said mirror result and an output of a second
6 state when said original result and said mirror result disagree, said second state
7 comprising an SEU error signal.

1 8. A method according to claim 7 comprising producing an output of the
2 second state from said comparison circuit in the absence of the original or the
3 mirror result.

1 9. A method according to claim 7 further comprising inhibiting production
2 of additional mirror results when said output is in the first state.

1 10. A method according to claim 9 further comprising performing an SEU
2 recovery routine in response to detection of an SEU error signal.

1 11. A method according to claim 10 further comprising storing the original
2 result and the mirror result in response to an SEU error signal, coupling the SEU
3 error signal to command production of a next original result and a next mirror
4 result, coupling said original result for comparison with said next original result by
5 said comparison circuit and coupling said mirror result for comparison with said
6 next mirror result by said comparison circuit and producing in said comparison
7 circuit a signal of the first state when at least one of the original result and next
8 original result or the mirror result and next mirror result match to allow use of a
9 result matching a next result by said processor.

1 12. A method according to claim 11 wherein allowing use comprises
2 transmitting the result to a processor bus.

1 13. A programmed medium which when executed on a processor
2 performs the steps of: executing an original and mirror instructions to produce an
3 original and a mirror result respectively to be compared in a redundancy routine,
4 and receiving signals indicative of a comparison by a radiation hardened
5 comparison circuit, and responding to an output of a first state from said
6 comparison circuit when said original result agrees with said mirror result to treat
7 the original result as true and responding to an output of a second state from said
8 comparison circuit when said original result and said mirror result disagree, said
9 second state comprising an SEU error signal, to treat the original result as not
10 true.

1 14. A medium according to claim 13 further performing the step of
2 inhibiting production of additional mirror results when said output is in the first
3 state.

1 15. A medium according to claim 14 further performing the step
2 performing an SEU recovery routine in response to detection of an SEU error
3 signal.

1 16. A medium according to claim 15 further performing the steps of
2 storing the original result and the mirror result in response to an SEU error signal,
3 coupling the SEU error signal to command production of a next original result
4 and a next mirror result, coupling said original result for comparison with said
5 next original result by said comparison circuit and coupling said mirror result for
6 comparison with said next mirror result by said comparison circuit and
7 responding to producing in said comparison circuit a signal of the first state when
8 at least one of the original result and next original result or the mirror result and
9 next mirror result match to allow use of a result matching a next result by said
10 processor.